

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Ronald DeShawn Blanton

Serial No.: To Be Assigned

Filed: Concurrently Herewith

For: METHODS FOR CHARACTERIZING, GENERATING TEST SEQUENCES FOR,  
AND/OR SIMULATING INTEGRATED CIRCUIT FAULTS USING FAULT  
TUPLES AND RELATED SYSTEMS AND COMPUTER PROGRAM PRODUCTS



May 25, 2001

Box PATENT APPLICATION

Commissioner for Patents


Washington, DC 20231

**INFORMATION DISCLOSURE STATEMENT  
CITATION UNDER 37 C.F.R. § 1.97**

Sir:

Attached is a list of documents on form PTO-1449 together with a copy of each identified document. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.97 and Section 609 of the MPEP.

Respectfully submitted,



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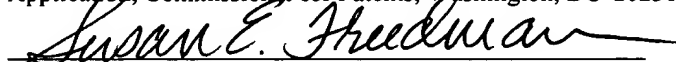
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Susan E. Freedman

Date of Signature: May 25, 2001



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